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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte WARD D. PARKINSON and ALLEN BENN

Appeal 2008-0651
Application 10/634,153
Technology Center 2800

Decided: June 3, 2008

Before KENNETH W. HAIRSTON, JOHN A. JEFFERY, and CARLA M. KRIVAK, *Administrative Patent Judges*.

JEFFERY, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 1-25. We have jurisdiction under 35 U.S.C. § 6(b). We affirm-in-part.

STATEMENT OF THE CASE

Appellants invented a method for forming an analog memory using a phase change material. Specifically, an analog memory is used to store analog information, such as audio and video information, radio signals, and other wireless signals. Using such an analog memory, the magnitude as an analog value is stored instead of a digitized value which can, among other things, reduce the cost of storage.[1] Claim 1 is illustrative:

1. A method comprising:
   forming an analog memory using a phase change material.

The Examiner relies on the following prior art references to show unpatentability:

Czubatyj '340	US 4,782,340	Nov. 1, 1988
Czubatyj '046	US 5,825,046	Oct. 20, 1998
Klersy	US 5,933,365	Aug. 3, 1999
Ovshinsky	US RE37,259 E	Jul. 3, 2001
Van Brocklin	US 6,879,525 B2	Apr. 12, 2005 (filed Oct. 31, 2001)

1. Claims 1-25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Ovshinsky.
2. Claims 1-25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Klersy.
3. Claims 1-25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Czubatyj '046.

[1] *See generally* Spec. 1:1-2:10.

4. Claims 1-17 and 19-25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Van Brocklin.
5. Claims 1-19 and 21-25 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Czubatyj '340.[2]

Rather than repeat the arguments of Appellants or the Examiner, we refer to the Briefs[3] and the Answer for their respective details. In this decision, we have considered only those arguments actually made by Appellants. Arguments which Appellants could have made but did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

OPINION

I. The Obviousness Rejections Based on Ovshinsky, Klersy, or Czubatyj '046

We first consider the Examiner's obviousness rejections of claims 1-25 over the disclosures of Ovshinsky, Klersy, or Czubatyj '046 (Ans. 4-9). In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. *See In re Fine*, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

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[2] The Examiner has withdrawn a rejection under 35 U.S.C. § 112 (Ans. 3). Therefore, that rejection is not before us.

[3] We refer to the most recent Appeal Brief filed October 16, 2006, and the Reply Brief filed March 26, 2007, throughout this opinion.

Discussing the question of obviousness of a patent that claims a combination of known elements, the Court in *KSR Int'l v. Teleflex, Inc.*, 127 S. Ct. 1727 (2007) explains:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill. *Sakraida* [*v. AG Pro, Inc.,* 425 U.S. 273 (1976)] and *Anderson's-Black Rock* [, *Inc. v. Pavement Salvage Co.*, 396 U.S. 57 (1969)] are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR, 127 S. Ct. at 1740. If the claimed subject matter cannot be fairly characterized as involving the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement, a holding of obviousness can be based on a showing that "there was an apparent reason to combine the known elements in the fashion claimed." *Id.* at 1740-41. Such a showing requires:

> some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. . . . [H]owever, the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ.

Id. at 1741 (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

If the Examiner's burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence.

Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. *See In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

Claims 1, 3-11, 13-15, 18-20, 21, 23, and 24

Regarding representative claim 1,[4] Appellants do not dispute the Examiner's findings with respect to the use of a phase change material in the cited prior art, but rather argue that the cited references do not disclose an "analog memory" since the references relate to *digital* – not analog – systems. Appellants emphasize that the term "analog memory" is defined in the Specification as "capable of storing the magnitude as an analog value instead of as a digitized value" (Reply Br. 2). According to Appellants, since the cited prior art teaches storing *states*, the references pertain to digital storage – not analog storage. While Appellants acknowledge that the term "analog storage" is used in the prior art, the term as used in that context nevertheless refers to converting the analog information to digital form, and storing the *digital* form of the information (App. Br. 12; emphasis added). These arguments apply for all three cited references (App. Br. 12-13).

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[4] Appellants argue all rejected claims together as a group for each rejection respectively. *See* App. Br. 12-14. Accordingly, we select claim 1 as representative for each rejection. However, since Appellants do present separate arguments for claim 2 (App. Br. 14), we treat this claim separately along with claims 12, 16, 17, 22, and 25 which recite commensurate limitations. *See* 37 C.F.R. § 41.37(c)(1)(vii).

Also, although Appellants indicate that all of the claims were rejected over the Van Brocklin and Czubatyj '340 references (App. Br. 10, 12), the Examiner did not reject all claims over these references, but rather rejected only those claims as indicated on page 3, *supra*, of this opinion. *See also* Ans. 9 and 11.

The Examiner takes the position that since the cited prior art states that memories can store both analog and digital information, it implies that either type of data (analog or digital) can be stored separately or together (Ans. 13).

The issue before us, then, is whether Appellants have shown that the Examiner erred in construing the prior art's teaching of a device that is capable of both analog and digital forms of information storage teaches or suggests an "analog memory" as claimed. For the following reasons, we conclude that Appellants have not shown error in the Examiner's interpretation.

Before turning to the prior art, we first construe the term "analog memory" and accordingly refer to Appellants' Specification for guidance.[5] Specifically, the Specification distinguishes digital information (i.e, in the form of digital states or bits of information) from "smoothly varying" analog information.[6] In this regard, the Specification notes that storing such analog information digitally requires a large number of samples (Spec. 1:7-17).

However, the Specification notes that, as an alternative, the "analog information may be stored in an analog memory *capable of* storing the magnitude as an analog value instead of as a digitized value....Storing the

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[5] *See Phillips v. AWH Corp.,* 415 F.3d 1303, 1321 (Fed. Cir. 2005) (en banc) ("[T]he specification is 'the single best guide to the meaning of a disputed term,' and...'acts as a dictionary when it expressly defines terms used in the claims or when it defines terms by implication.'") (internal quotation marks and citations omitted).

[6] According to the Specification, "[a]nalog information may include the characteristics of a non-periodic wave such as a sound wave" (Spec. 1:8-10). The Specification further cites examples of storable analog information to include audio and video information, radio signals, and other wireless signals (Spec. 2:7-9).

analog value for each time slice in each memory locations [sic] instead of the digitized value…can reduce the cost of storage" (Spec. 1:18-2:2; emphasis added).

Based on this discussion, we find that Appellants have, in effect, implicitly defined the term "analog memory" as a memory that is *capable of* storing analog values. Appellant's characterization of an "analog memory" as "one that stores an analog value as a magnitude and not as a digitized value" (Reply Br. 2) may be true when the memory is actually loaded with data. But Appellants argument is simply not commensurate with the scope of the limitation. That is, a memory need not actually have analog data stored therein to constitute an "analog memory." Rather, the memory need only be *capable of* storing analog data.

With this construction, we turn to the prior art. Ovshinsky describes in the Background section of the reference a non-volatile, thin-film electronic memory device known as an Ovonic EEPROM. Ovshinsky notes that this device is capable of *both analog and digital* forms of information storage (Ovshinsky, col. 1, ll. 20-28; emphasis added).

Ovshinsky further details the use of phase change materials for electronic memory applications, and notes that switching such materials in earlier patents can be incremental to provide a "grey scale" represented by a multiplicity of conditions spanning the completely amorphous and crystalline states (Ovshinsky, col. 1, ll. 36-60).

Additionally, Ovshinsky notes that the dynamic range of resistances allows for broad grey scale and multilevel analog memory storage that allows for storing multiple bits of binary information in a single memory cell. This multilevel storage is accomplished by mimicking multiple bits of

binary information in pseudo-analog form and storing this analog information in a single memory cell (Ovshinsky, col. 20, ll. 56-67).

While we agree with Appellants (App. Br. 12) that the passage in column 20 indicates that grey scale and multilevel memory storage allows for binary information to be stored, we do not agree that this description necessarily limits the interpretation of analog information referred to in the Background section pertaining to the Ovonic EEPROM.

First, as we noted above, this EEPROM is capable of *both analog and digital* forms of information storage (Ovshinsky, col. 1, ll. 20-28). Secondly, Ovshinsky notes with respect to the EEPROM that "[d]igital storage can be either *binary* (one bit per memory cell) or *multi-state* (multiple bits per cell)" (Ovshinsky, col. 1, ll. 28-30; emphasis added). While the analog form of information storage is not further detailed in this context, digital storage is described as binary or multi-state – states that are clearly distinguished from analog forms.

Based on this distinction, ordinarily skilled artisans would have reasonably inferred from this passage that an analog form of information storage would therefore *not* involve storing discrete bits (or a single bit) in a cell, but rather involve storing other forms of data (i.e., analog). In our view, the fact that this memory is stated to be capable of storing analog forms of information reasonably suggests that analog values are capable of being stored if they are so employed. Moreover, we agree with the Examiner (Ans. 13) that ordinarily skilled artisans would have also recognized from this teaching that either type of data (analog or digital) could be stored separately or together.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of representative claim 1 based on the disclosure of Ovshinsky. We therefore sustain the Examiner's rejection of that claim, and claims 3-11, 13-15, 18-20, 21, 23, and 24 which fall with claim 1.

Since Appellants repeat the same arguments for each rejection (i.e., the three separate obviousness rejections citing Ovshinsky, Klersy, and Czubatyj '046, respectively (App. Br. 12-13)), Appellants likewise have not persuaded us of error in the Examiner's rejections of representative claim 1 based on the disclosures of Klersy or Czubatyj '046 for similar reasons. Therefore, we will also sustain the Examiner's rejections of representative claim 1 based on these references, and claims 3-11, 13-15, 18-20, 21, 23, and 24 which fall with claim 1.

II. The Obviousness Rejection Based On Van Brocklin
Claims 1, 3-11, 13-15, 19, 20, 21, 23, and 24

We now consider the Examiner's obviousness rejection of claims 1-17 and 19-25 over Van Brocklin (Ans. 9-11). Regarding representative claim 1, Appellants argue that since Van Brocklin stores *states*, it pertains to digital storage – not analog storage (App. Br. 13).

The Examiner notes that Van Brocklin's changeable resistance (phase change material) stores the magnitude of information representing data in analog form. According to the Examiner, since current that is read out from each cell is already in analog form, any amount of analog data can be stored by merely varying the magnitude of the applied voltage. The Examiner further notes that the stored current value read out from the memory cell in Van Brocklin continuously varies as shown in Figure 4 (Ans. 9-10, 13-14).

The issue before us, then, is whether Van Brocklin reasonably teaches or suggests an "analog memory" as claimed. For the following reasons, we find that it does.

At the outset, our previous discussion construing the term "analog memory" applies equally here and we therefore incorporate that discussion by reference. Turning to the prior art, Van Brocklin discloses an integrated circuit with an array of state-change devices and decoder circuits for selecting a particular state-change device (Van Brocklin, Abstract). A feedback write method is used to alter a state-changeable memory cell such as, among other things, a phase change device (Van Brocklin, col. 2, ll. 44-47; col. 3, l. 50 - col. 4, l. 2). This feedback method – which can be continuous or discretely implemented – takes advantage of the current/voltage curves of programmable memory cells that have a continuous change of state between a non-programmed state and a programmed state (Van Brocklin, col. 2, ll. 55-66).

As shown in Figure 1 of Van Brocklin, the non-programmed state 12 has a particular relationship between the state-change device's voltage and current. As the memory cell voltage is held at the program voltage 22, the resistance of the state-change device decreases, thus causing less voltage to drop across the device. This change in resistance ultimately tapers to a fixed value, and the state-change device is then considered to be in a fully programmed state 18. However, Van Brocklin's technique allows for stopping the programming process before the state-change device completes its transition to the fully programmed state. These "partial programmed" states are shown in Figure 1 as first and second partial programmed states 14, 16, respectively. Although only four states of the memory cell are

shown in Figure 1, any amount of states could be implemented (Van Brocklin, col. 4, ll. 23 - col. 5, l. 17; col. 5, ll. 32-35; Fig. 1).

Figures 3 and 4 detail a preferred implementation of this technique. During programming, voltage source 70 is set to the program voltage 22 (shown as Signal B in Figure 4) which is applied across control element 54 and state-change device 52 of the selected memory cell 56. As shown by Signal C of Figure 4, the current through the state-change device (or the voltage across sense resistor 74) increases steadily due to the altered state of the state-change device. When Signal C reaches a predetermined value, current is disabled through the state-change device and programming is stopped (Van Brocklin, col. 7, ll. 34-65; Figs. 3 and 4).

Based on this functionality, we find that such a memory unit would have reasonably suggested to ordinarily skilled artisans that it is capable of functioning as an "analog memory." Furthermore, we find the detected current and voltage values of each memory cell to be analog values that are stored. Therefore, we agree with the Examiner (Ans. 14) that while Van Brocklin may convert these analog values into digital values *as the end result* (i.e., via decoder 90[7]), the memory cell structure itself is nonetheless capable of storing analog values using a phase change material and therefore fully meets an "analog memory" as claimed. That these analog values ultimately represent a particular programmed state does not detract from the fact that these values are nevertheless stored to make such a determination.

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[7] Decoder 90 is coupled to sense resistor 74. The decoder is preferably an analog to digital converter that is used to decode the programmed state of the memory cell (Van Brocklin, col. 7, ll. 27-32; Fig. 3).

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of representative claim 1 over the disclosure of Van Brocklin. Therefore, we will sustain the Examiner's rejection of that claim, and claims 3-11, 13-15, 19, 20, 21, 23, and 24 which fall with claim 1.

III. The Obviousness Rejection Based on Czubatyj '340
Claims 1, 3-11, 13-15, 18, 19, 21, 23, and 24

We now consider the Examiner's obviousness rejection of claims 1-19 and 21-25 over Czubatyj '340 (Ans. 11-13). Appellants argue that while Czubatyj '340 discusses electrically detectable forms and teaches "what might be loosely and incorrectly called storing analog information," the reference nonetheless does so by digitizing that information (App. Br. 13-14).

The Examiner notes that Czubatyj '340 teaches the use of a phase change material to store data by continuously varying resistance values to represent data levels. According to the Examiner, Czubatyj '340 states that information can be stored in analog form *or any other electrically detectable form* (Ans. 12; emphasis in original). This teaching, the Examiner contends, would have suggested to ordinarily skilled artisans the alternative of using applied currents or voltages to obtain cell resistance values (Ans. 11-12).

The issue before us, then, is whether Czubatyj '340 reasonably teaches or suggests an "analog memory" as claimed. For the following reasons, we find that it does.

At the outset, our previous discussion construing the term "analog memory" applies equally here and we therefore incorporate that discussion

by reference. Turning to the prior art, Czubatyj '340 in the Background section discusses typical thin film electronic arrays 50 that are shown in Figures 1 through 3. The arrays comprise electronic cells 58 that may include, among other things, a memory unit and phase change material. Cells are accessed or addressed by appropriate signals which may be voltage or current waveforms of varying amplitudes applied substantially simultaneously to associated conductors. The cells may receive and store information present in the applied signals via information-bearing means 62 (Czubatyj '340, col. 1, l. 58 - col. 2, l. 30; col. 2, l. 60 - col. 3, l. 2; Figs. 1-3). According to Czubatyj '340, an "information-bearing means" is "any means known or hereafter created for receiving or *storing information present in the applied signals or waveforms*, or for imparting information to the applied signals or waveforms" (Czubatyj '340, col. 2, ll. 27-30; emphasis added).

Based on this functionality, we find such a memory unit that stores information present in the applied signals or waveforms would have reasonably suggested to ordinarily skilled artisans that such a memory is capable of functioning as an "analog memory."

Significantly, Czubatyj '340 expressly states that the information stored in the information-bearing means may be either (1) in digital form such as a binary value, e.g., logical "one" or logical "zero," or (2) an analog value *such as* a "gray-scale" value, *or any other electrically detectable form* (Czubatyj '340, col. 2, ll. 30-34; emphasis added).

We find this teaching particularly relevant to the issue before us. In this discussion, Czubatyj '340 clearly distinguishes digital forms of information from analog values. That is, digital forms can be binary values

(e.g., logical ones and zeroes). Analog values, however, may not only include (and are not limited to) "gray-scale" values, the information may also include "any other electrically detectable form."

Therefore, even if we assume, without deciding, that the gray-scale values are in effect digitized analog forms as Appellants argue (App. Br. 13), the reference also includes "any other electrically detectable form" of information – forms which clearly suggest analog information. In our view, this catch-all category would have reasonably suggested to ordinarily skilled artisans a wide variety of analog values storable in the information-bearing means. Moreover, skilled artisans would reasonably conclude that "any other electrically detectable form" of information is, in effect, distinguished from "gray-scale" values in the context of the discussion as a separate and distinct form of information.

For the foregoing reasons, Appellants have not persuaded us of error in the Examiner's rejection of representative claim 1 based on Czubatyj '340. Therefore, we will sustain the Examiner's rejection of that claim, and claims 3-11, 13-15, 18, 19, 21, 23, and 24 which fall with claim 1.

Claims 2, 12, 16, 17, 22, and 25

We will not, however, sustain the Examiner's rejections of claims 2, 12, 16, 17, 22, and 25. While we find that the cited prior art teaches or suggests an analog memory as noted above, we fail to find any reasonable teaching or suggestion to *selectively enable* either digital or analog data to be stored in such a memory as recited in claims 2, 12, and 22. Moreover, the prior art does not teach or suggest a circuit to enable such a storage selection as recited in claims 16, 17, and 25.

For the foregoing reasons, we will not sustain the Examiner's rejections of claims 2, 12, 16, 17, 22, and 25.

DECISION

We have sustained the Examiner's rejections with respect to claims 1, 3-11, 13-15, 18-21, 23, and 24. We have not, however, sustained the Examiner's rejections of claims 2, 12, 16, 17, 22, and 25. Therefore, the Examiner's decision rejecting claims 1-25 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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